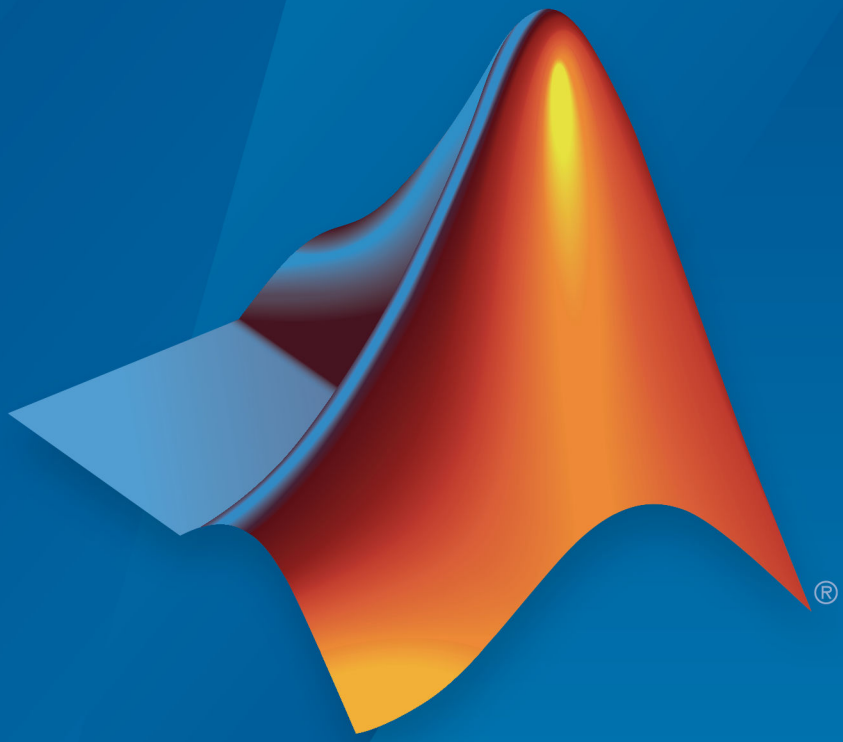
SoC Blockset™ Release Notes



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R2019b

R2019a

R2019b

Version: 1.1

New Features

Bug Fixes

Proxy Task Block: Model the effect of a task in an application without an explicit task implementation

The Proxy Task block models the effect of a task on an application without defining the implementation of the task. You can configure the block execution timing by using the Task Manager block. The Proxy Task block is a placeholder for a task to be developed.

Testbench Task Block: Model the effect of a external task competing for resources with an application

The Testbench Task block models the effect of a task in an external application competing for execution resources with the tasks in an application. You can configure the block execution timing by using the Task Manager block.

Playback control behavior changed for Logic Analyzer in referenced models

When you use the **Logic Analyzer** in a referenced model, the playback controls in the Logic Analyzer now match the playback controls of the last model you interacted with that logs data to the scope. For example, if you opened the Logic Analyzer from a model referenced by another model with the Model block, the run button  in the scope runs the top level model. If the referenced model is opened as a top model, the run button runs the referenced model in isolation.

Updates to supported software

SoC Blockset™ now supports to these software versions. For a full list of supported software, see “Supported Third-Party Tools and Hardware”.

- Xilinx® Vivado® 2018.3
- Intel® Quartus® Prime 18.1

IO Data Source Block: Read data from a recorded data file at the same time interval at which it was recorded on the hardware board

You can now use the IO Data Source block to read data from a recorded data file at the same time interval as it was recorded on the hardware board.

When you enable the event port of the IO Data Source block and connect it to the Task Manager block, the IO Data Source block reads event signals and generates them on the event port as they were recorded in the recorded data file. Previously, the IO Data Source block generated events based on the sample time specified on the block mask.

This feature enables you to see the real behavior of the data from hardware I/O peripherals in Simulation.

Kernel Profiler: Monitor and record execution times of tasks with LTTng

You can use a Kernel profiler to monitor and record model-related processes and threads running on the Linux of your hardware board without instrumenting code.

Hardware Memory Diagnostics: View additional latencies and data overflow information from FPGA execution

In addition to viewing **Burst request to first transfer complete** latency information from a design running on field programmable gate array (FPGA), you can now view **Burst execution** and **Burst last transfer to complete** latencies information. This feature is similar to that of “Simulation Performance Plots”.

You can also collect and view data overflow that occurred in bandwidth, burst, and latency memory diagnostics metrics.

R2019a

Version: 1.0

New Features

Introducing SoC Blockset: Design, evaluate, and implement SoC hardware and software architectures

SoC Blockset provides Simulink® blocks and visualization tools for modeling, simulating, and analyzing hardware and software architectures for ASICs, FPGAs, and systems on a chip (SoC). You can build your system architecture using memory models, bus models, and I/O models, and simulate the architecture together with the algorithms.

SoC Blockset lets you simulate memory and internal and external connectivity, as well as scheduling and OS effects, using generated test traffic or real I/O data. You can quickly explore different system architectures, estimate interface complexity for hardware and software partitioning, and evaluate software performance and hardware utilization.

SoC Blockset exports reference designs for Xilinx and Intel FPGA devices and SoC platforms, including Zynq®-7000, UltraScale+™, and Intel SoC FPGAs. These reference designs can be used with Xilinx and Intel design tools.

SoC Blockset Support Package for Xilinx Devices: Generate, build, and deploy reference designs on Xilinx devices

The SoC Blockset Support Package for Xilinx Devices with Embedded Coder® or HDL Coder™ can export reference designs for Xilinx FPGA devices and SoC platforms. These reference designs can be used with Xilinx design tools.

The support package helps to automate integration, execution, and verification of reference designs for the SoC platforms, including Xilinx Artix®-7, Xilinx Kintex®-7, XilinxZynq, and XilinxZynqUltraScale+.

SoC Blockset Support Package for Intel Devices: Generate, build, and deploy reference designs on Intel devices

The SoC Blockset Support Package for Intel Devices with Embedded Coder or HDL Coder can export reference designs for Intel FPGA devices and SoC platforms. These reference designs can be used with Intel design tools.

The support package helps to automate integration, execution, and verification of reference designs for the SoC platforms, including Intel Arria® 10 and Intel Cyclone® V.